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WILLIAMS, MORGAN & AMERSON
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER	
LANIER, BENJAMIN E	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/852,942
Filing Date: May 10, 2001
Appellant(s): STRONGIN ET AL.

Mark W. Sincell
Reg. No. 52,226
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10 November 2005 appealing from the Office action mailed 24 June 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,286,097	CHANG	9-2001
5,844,986	DAVIS	12-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4, 10-16, 18-20, 23-26, 28, 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang, U.S. Patent No. 6,286,097. Referring to claim 1, 12, Chang discloses a computer system for accessing read only memory (ROM) wherein the computer system comprises a main processor (Fig. 8, 310), a bridge coupled to the processor (Fig. 8, 322), a memory selectably coupled to the bridge and the processor (Fig. 8, 350), a switching mechanism coupled between the memory of each of the processor and the bridge, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the bridge to the memory (Fig. 8, 325 & Abstract).

Referring to claims 2-4, Chang discloses that the booting control circuit (Fig. 8, 323) sends out a signal when the system is booting up, which allows the processor access to the ROM so that the necessary boot information can be shadowed into main memory. After the transfer, the boot control circuit signals to the switching mechanism that the boot process has completed and ROM access is passed to the peripherals (Col. 3, lines 13-27), which meets the limitations of control logic coupled to the switching mechanism for controlling changes between the first state and the second state, a second bridge coupled between the bridge and the processor, wherein the control logic is comprised within or controlled by the second bridge, wherein the control logic is comprised within or controlled by the processor (Fig. 8, 300).

Referring to claim 10, Chang discloses that the memory and the bridge are coupled to an I/O bus (Fig. 8, 350, 322B, 324), wherein the bridge further comprises I/O bus interface logic for communicating to the I/O bus (Fig. 8, 324, 322B), wherein the processor further comprises I/O bus interface logic for communicating to the I/O bus (Fig. 8, 310), wherein the switching mechanism is coupled to the I/O bus (Fig. 8, 325B, 325C), wherein the processor is coupled to

the switching mechanism through the I/O bus interface logic (Fig. 8, 310, 322B, 324, 325B, 325C), wherein the first state comprises the I/O bus interface logic of the processor being configured to communicate with the memory over the I/O bus (Col. 3, lines 13-27, Fig. 8 300), and wherein the second state comprises the I/O bus interface logic of the bridge being configured to communicate with the memory over the I/O bus (Col. 3, lines 18-27, Fig. 8 300).

Referring to claim 11, Chang discloses that the second I/O bus comprises an LPC bus (Fig. 8, 324).

Referring to claim 13, Chang discloses that the ROM is a BIOS ROM (Col. 1, line 53).

Referring to claims 14, 18-20, 23, 24, 28, 29, Chang discloses a computer system comprising a processor (Fig. 8, 310), a memory (Fig. 8, 350), and a first device (Fig. 8, 322), wherein the processor is operably coupled to the first device, and the first device is operably coupled to the memory (Fig. 8, 310, 322, 325, 350 & Abstract). Coupling the processor and the memory using a switching mechanism (Fig. 8, 325), wherein the switching mechanism is configured to operate in a first state operably coupling the first device to the memory and a second state operably coupling the processor to the memory (Col. 3, lines 13-27), switching the computer system into the second state, thereby operably coupling the memory to the processor using the switching mechanism (Col. 3, lines 13-18), reading from memory in the second state (Col. 4, line 65 – Col. 5, line 2), means for controlling the means for switching (Fig. 8, 323).

Referring to claims 15, 25, Chang discloses the processor is coupled to the first device through at least a system bus (Fig. 8, 310, 322), wherein the first device is coupled to the memory through a first I/O bus (Fig. 8, 322B, 324, 325B, 325C, 350), wherein coupling the

processor and the memory using the switching mechanism comprises coupling the processor to the first I/O bus through the switching mechanism (Fig. 8, 325 A-C).

Referring to claims 16, 26, Chang discloses that the ROM contains BIOS information and that when the computer system boots up the processor accesses the programs stored on the ROM to boot the computer system (Col. 4, line 63 – Col. 5, line 5), which meets the limitation of the second state comprises booting the computer system, wherein the memory comprises a ROM, and wherein reading from the memory comprises reading BIOS information from the ROM.

Claims 5-9, 17, 21, 22, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, U.S. Patent No. 6,286,097, in view of Davis, U.S. Patent No. 5,844,986. Referring to claim 5-9, 17, 21, 22, 27, Chang discloses a computer system for accessing a BIOS ROM (Col. 1, line 53) wherein the computer system comprises a main processor (Fig. 8, 310), a bridge coupled to the processor (Fig. 8, 322), a memory selectably coupled to the bridge and the processor (Fig. 8, 350), a switching mechanism coupled between the memory of each of the processor and the bridge, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the bridge to the memory (Fig. 8, 325 & Abstract). A second bridge coupled between the bridge and the processor (Fig. 8, 310, 322, 323), wherein the second bridge is coupled to the processor through the local bus (Fig. 8, 310, 323), wherein the second bridge is coupled to the bridge through the first I/O bus (Fig. 8, 323, 322B, 324, 325A-C). Chang does not disclose that the ROM is a secure ROM accessible through a crypto-processor. Davis discloses a secure BIOS ROM that is housed within a crypto-processor so that when the computer system boots, the main processor issues a read request for an address corresponding to the BIOS program. The cryptographic processor

responds to that request with the associated BIOS instruction (Col. 3, lines 30-34). The main processor processes the data and BIOS instructions (Col. 3, lines 34-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the secure BIOS ROM of Davis in the ROM accessing system of Chang in order to protect the BIOS ROM for potential viruses and corruption as taught in Davis (Col. 1, lines 62-67).

(10) Response to Argument

Appellant's argument that "Chang does not describe or suggest a switching mechanism that provides a first state providing access from a processor to a memory and a second state providing access from the device to the memory, i.e., the second state permits the device to access the same memory as the processor has access to in the first state," is not persuasive because Chang discloses a computer system for accessing read only memory (ROM) (Figure 8, element 350). The claimed processor is met by the main processor of Chang (Figure 8, element 310). The claimed bridge coupled to the processor is met by element 322 of Figure 8. Element 322 is coupled to the main processor (310) through the main control circuit (Figure 8, element 321). The claimed switching mechanism coupled between the memory and each of the processor and the bridge is met by element 325 of Figure 8. Element 325 is coupled to the memory of Chang through individual connections with switching circuits 325A-325C that are shown in Figure 8. Element 325 is coupled to the main processor through the main control circuit (322) and booting control circuit (Figure 8, element 323). Element 325 is directly coupled to element 322 as shown in Figure 8. The claimed first state that provides access from the processor to the memory is shown in Figure 8 as element B of the individual switching circuits 325A-325C, connecting the ROM (350) to the booting control circuit (323), which is coupled to the main

processor as mentioned above. The claimed second state providing access from the bridge to the memory is shown in Figure 8 as element A of the individual switching circuits 325A-325C, connecting the ROM (350) to various elements of element 322. The individual switching elements 325A-325C are detail in Figures 4-5 and discussed in Chang on column 5, line 57 through column 6, line 22. This portion of Chang, along with Figures 4-5, details how the switches operate. Each individual switching circuit (325A-325C in Figure 8 or individually in Figures 4-5) has two sets of electronic switches (i.e. first electronic switches 411-41N and second electronic switches 421-42N for Figure 4, and 511-51N and 521-521N for Figure 5).The first electronic switch corresponds to input A from Figure 8 and is identified in that fashion for Figures 4-5, which the second electronic switch corresponds to input B from Figure 8 and is similarly identified in that fashion for Figures 4-5. When the selection signal S is in the high level, the first electronic switches 411-41N turn ON, while the second electronic switches 421-42N turn OFF (Figure 4 & Col. 5, line 67 – Col. 6, line 3). On the other hand, when the selection signal S is in the low level, the first electronic switches 411-41N turn OFF, while second electronic switches 421-42N turn ON (Figure 4 & Col. 6, lines 3-5). Column 6, lines 6-22 detail similar functionality from Figure 5. This shows how Chang meets the limitations of first and second states because these individual switching circuits (Figure 8, 325A-325C) toggle between inputs A or B, which are coupled to elements 322 and the main processor 310 respectively, as shown above. Therefore, when an individual switching circuit is switched to input B, the claimed limitation of a first state is met because the main processor is connected to the ROM through the B connection in the individual switching circuit. Similarly, when the individual switching circuit

is switched to input A, the claimed limitation of a second state is met because element 322 is connected to the ROM through the A connection in the individual switching circuit.

Appellant appears to be arguing that the Chang reference does not have dedicated connections between the claimed elements, however, the claims to not require such connections to be present in the prior art. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant's arguments with respect to the combination of the Chang and Davis references mirror the previous arguments, relying on Appellant's belief that claims 1-4, 10-16, 18-20, 23-26, and 28-29 are not anticipated by Chang as the sole rationale for Appellant's argument, that "the cited reference fail to provide any suggestion or motivation to modify the prior art of record to arrive at the claimed invention." Support for the anticipated rejection of claims 1-4, 10-16, 18-20, 23-26, and 28-29, in view of Chang, has been presented above. The details of Chang are disclosed above. Chang does not disclose that the ROM is a secure ROM accessible through a crypto-processor. Davis discloses a secure BIOS ROM that is housed within a crypto-processor so that when the computer system boots, the main processor issues a read request for an address corresponding to the BIOS program. The crypto-processor responds to that request with the associated BIOS instruction (Col. 3, lines 30-34). The main processor processes the data and BIOS instructions (Col. 3, lines 34-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the secure BIOS ROM of Davis in the ROM accessing system of Chang in order to protect the ROM from potential viruses and corruption as taught in Davis (Col. 1, lines 62-67).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Benjamin E. Lanier

Conferees:

Kim Vu KV

Christopher Revak

CHRISTOPHER REVAK
PRIMARY EXAMINER